REMARKS

Claims 1-18 were previously pending in the present application. Claims 1-18 were each rejected. Claim 19 is newly added in this paper. The originally-filed claim set included 18 claims but inadvertently listed two claims 3 and therefore the claim numbering only went up to claim 17 (1-3, 3-17). The second one of the original claims 3 has been cancelled and rewritten as newly added claim 18. As such, even though claims 18 and 19 appear as "newly added" only newly added claim 19 was not present in the originally-filed application. Claims 1, 16 and 17 are being amended.

Applicants respectfully request re-examination and reconsideration of claims 1-18 and allowance of each of presently pending claims 1-19.

I. Claim Objections

In subject Office action, specifically in paragraph 2, claims 3-17 were objected to because the original claim set included two claims that were consecutively numbered as claim 3. The latter of the originally filed claims 3 has been canceled and added as newly added claim 18. The pending claim set now includes claims 1-19. The claim objection should therefore be withdrawn.

II. Objection to the Specification

In the subject Office action, specifically in paragraph 3, the Examiner indicated that the title of the invention is not descriptive. Responsive to the Examiner's suggestion, the original title has been essentially replaced with the title proffered by the Examiner: Method of Making a Multiple Gate Electrode on a Semiconductor Device.

As amended, the title is now suitably descriptive and indicative of the invention to which the claims are directed and the objection to the specification should therefore be withdrawn.

Claim Rejections under 35 U.S.C. § 102

In the subject Office action, specifically in paragraph 2, claims 1, 3-5, 8-9 and 14-18 were rejected under 35 U.S.C § 102(e) as being anticipated by Clark et al. (U.S. Pat. No. 6,767,793), hereinafter "Clark". While claims "1, 3-5, 8-9 and 14-18" were rejected in this section, Applicants understand that, due to the claim discrepancy as discussed with respect to the claim objections above, these claim rejections apply to the claims numbered by Applicants as 1, 3, 3, 4, 7-8, and 13-17. Applicants respectfully submit that these claim rejections are overcome for the reasons set forth below.

The claims rejected under 35 U.S.C. § 102(e) include independent claims 1 and 16, the only independent claims that were previously pending.

Independent claim 1 has been amended and now recites the features of "a semiconductor device that has been previously coated with a thin film of gate dielectric *on the top* and the opposed sides of the semiconductor device". Amended independent claim 1 also recites the feature of "coating a layer of gate electrode material over top and past the opposed sides of a semiconductor device . . . planarizing *the layer* of gate electrode material to a substantially planar *surface of the gate electrode material that extends past each of the opposed sides*".

Independent claim 16 (apparently considered to be claim 17 by the Examiner due to applicants' claim numbering error, but identified as claim 16 in the filed application)

has been amended and recites the features of: "a projecting fin coated with a gate dielectric film *over top* and opposed sides of the fin". Amended independent claim 16 also recites the feature of: "the multiple gate electrode formed of *a layer of gate electrode material* and having a substantially planar surface extending over the top and past each of the opposed sides of the fin".

The semiconductor device 155 of Clark does not contain a thin film of gate dielectric on opposed sides of the designated semiconductor device 155, much less a gate dielectric on opposed sides and the top, as in the claimed invention. Hard mask 100 is disposed over the top of Clark's semiconductor device 155 in Figure 15. Hard mask 100 is of increased thickness and is clearly distinguished from a gate dielectric as easily appreciated by one of ordinary skill in the a. Hard mask 100 cannot and does not serve as a gate dielectric. Furthermore, feature 100 is consistently and only referred to as "hard mask 100". Clark therefore does not teach the feature of the thin film gate dielectric extending over top of the semiconductor device, as recited in claims 1 and 16 of the claimed invention. It is because of the gate dielectric extending over the top as well as sides of the semiconductor device of applicants' invention, that an advantage is achieved - a multiple gate electrode with an increase channel area (including the top and sides of the semiconductor device). Applicants respectfully submit that Clark, in fact, teaches away from a gate dielectric formed over the top of the device because hard mask 100 is required for subsequent processing operations and therefore could not be replaced with a gate dielectric. As such, Clark does not *suggest* the feature of the thin film gate dielectric extending over top of the semiconductor device and claims 1 and 16 therefore includes features not taught or suggested by Clark. Moreover, Clark

only teaches a thin film of gate dielectric ("*gate oxide 40*") on one side of the illustrated semiconductor device 155, not on each of the opposed sides as in claims 1 and 16. Clark makes the point to distinguish "oxide 150", formed on the left hand side of semiconductor device 155, from a gate oxide when Clark recites "gate oxide 40, hard mask 100, oxide 150", at col. 5, line 35.

Clark also does not teach or suggest the feature of coating a layer of gate electrode material over top and sides of a semiconductor device and planarizing the layer of gate electrode material to a substantially planar surface of the gate electrode material that extends over the top and past the opposed sides of the semiconductor device, as does the claimed invention in claims 1 and 16.

Clark, in sharp contrast, includes a planar upper surface 170 of Figure 17 that necessarily consists of **two** materials that intersect over the top of body 155, neither of which extend past each of the opposed sides of body 155. Film 160, identified by the Examiner as the gate electrode material, does not extend past the right hand side of the semiconductor device, body 155. The planarized layer shown in Figure 17, therefore does not consist of **a** layer of gate electrode material and a planar surface that extends past each of the opposed sides of the semiconductor device as does the claimed invention. Rather, the planar upper surface 170 shown in Figure 17 of Clark is necessarily formed of two distinct materials: first polysilicon 50 and second polysilicon 160 that intersect over body 155. The two materials are clearly distinguished: ". . . planar upper surface 170, as shown in Fig. 17. Since the first polysilicon 50 was an N+ doped polysilicon, the second polysilicon 160 is preferably a P+ polysilicon." column 5, lines 42-45 of Clark. Moreover, a study of the Clark processing sequence (Figs. 3-17)

teaches the inventive concept and shows that Clark *requires* two different films disposed over the structure. Clark therefore doesn't suggest and cannot use a single gate material or produce a single planar surface from a single gate material that extends past both sides of the semiconductor device as in the claimed invention as recited in independent claims 1 and 16. Claims 1 and 16 therefore include further features not taught or suggested by Clark.

Independent claims 1 and 16 (rejected as claim 17 by the Examiner) therefore include multiple features that distinguish Applicants' invention from Clark and the rejection of claims 1 and 16/17 under 35 U.S.C. § 102 should be withdrawn.

Each of the rejected dependent claims depend from amended independent claims 1 and 16/17 and therefore incorporate the distinguishing features of their base claims. Therefore the rejection of claims 1, 3-5, 8-9 and 14-18 under 35 U.S.C § 102(e) as being anticipated by Clark, should be withdrawn.

III. Claim rejections under 35 U.S.C § 103

In the Office action, specifically in paragraph 4, claims 2, 6-7 and 10-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Clark as applied to claim 1 and further in view of Fried et al. (U.S. Pat. No. 6,657,252) and Yu (U.S. Pat. No. 6,648,662). Again, due to the claim numbering discrepancy described above, this rejection refers to the claims numbered 2, 5, 6 and 9-12 of the originally filed claim set. Applicants respectfully submit that these claim rejections are overcome based on the reasons set forth below.

The cited reference of Yu has apparently been relied upon for teaching the application of a photoresist mask and the cited reference of Fried has apparently been relied upon for disclosing various types of gate dielectric materials. Neither of the cited references of Yu or Fried makes up for the above-stated deficiencies of Clark, however. Neither Yu nor Fried teaches or suggests a gate oxide film that extends over sides and the top of the semiconductor device. Since claim 1 is distinguished from Clark as above and since rejected claims 2, 6-7 and 10-3 depend from claim 1, the claim rejections under 35 U.S.C § 103(a), as being unpatentable over Clark as applied to claim 1 and further in view of Fried et al. and Yu, should therefore be withdrawn.

IV. Claim 19

Claim 19 has been added to further point out distinguishing aspects of the applicants' invention and recites features that distinguish applicants invention from the references of record. Claim 19 is therefore in allowable form.

CONCLUSION

Based on the foregoing, each of claims 1-19 is in allowable form and the application is therefore in condition for allowance, which action is expeditiously and respectfully requested by applicants.

Respectfully submitted,

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